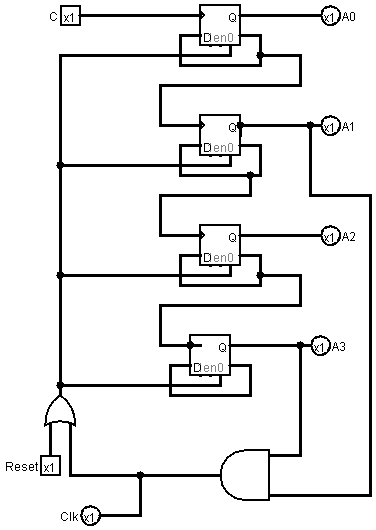
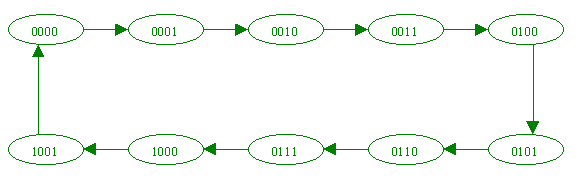
**PROBLEM STATEMENT**

DESIGN A 2- DIGIT 7 SEGMENTS DISPLAY USING TWO CASCADABLE COUNTERS WHICH DISPLAYS WITH EACH CLOCK CYLE, 0-1-2--------90-0------.

# # CIRCUIT FOR THE COUNTER:-



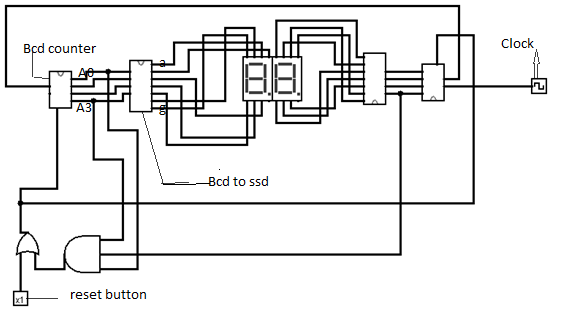
STATE DIAGRAM:



Counter’s Analysis: The circuit includes a 4-Bit Binary Ripple Counter with positive edge-triggered D flip-flops. A(0), A(1), A(2) and A(3) are the values generated by the counter where A(0) is the least significant bit. The complemented output of each flip-flop is given as its input and also as the clock input of the higher order flip-flop.

The counter is initialised by the reset button to 0000 and then the counter counts from 0000 to 1111 but here, we are restricting it till 1001. So as soon as the present state becomes 1010 , the reset for the flip flops becomes 1 and reset’s the output to 0000 .This is done by ANDing the A(1) and A(3) output of the flip flops so as to reset it after 1010 and providing it to the or gate with the reset button .So that the circuit can be reset to 0000 by either the reset button or the when the output is 1010.

#CIRCUIT FOR THE DISPLAY:

Display Circuit Analysis: The circuit consists of two Binary to Seven Segment Display converter and two counters one for the display of one’s digit and other for ten’s digit. The clock for the ten’s digit counter is the ANDed output of A(1) and A(3) of one’s digit counter so as change the ten’s digit only when the one’s digit has ran from 0 to 9 and is going to be reset. To reset the display again to 00 after displaying 90 we have used the reset which is the obtained by ORing the reset button and ANDed output of A(0) of one’s digit counter, A(0) and A(3) of ten’s digit counter. When the circuit displays 90 ,the next state it will display is 91 and since we want to display 00 again and follow the loop ,so when ten’s digit counter displays 9 and one’s digit counter becomes 1 we reset the flip flops by the ANDed output .Thus the display displays digits from 0-1-2----90 and then follows the loop back again.

Discussion: The IC 74HC74 used for the D flip flops in the counter has active low preset and clear and therefore the hardware involves NOT gate IC (7406) where the output of the OR gate(the one which is directly connected to the reset inside the counter) is complemented, so as to give active low input to the reset of 74HC74.The seven segment display IC 74LS47 used in the circuit has complemented a to g outputs and therefore Common Anode Led Displays have been used.

Conclusion: The circuit is capable of displaying 0-1-2------90-0----- via just two inputs for the circuit one being the reset button (which when kept high will reset the circuit to 00 display) and the other being the clock input (1 Hz preferably).

References :

1.Digital Design ,Fourth Edition ,M.Marris Mano and Michael D.Ciletti

2.Engineering Digital Design,Richard F.Tinder